Fig. 3 is a circuit configuration diagram showing a semiconductor integrated circuit according to the second embodiment of the present invention. This is an example in which the function of the logic gate for fixing the output signal to logic circuit g104 described in the first embodiment is incorporated into the inside of the MUX-type scan FF. In this configuration, the output terminal is divided into a scan-out terminal and a logic output terminal. Further, before the logic output terminal, a 2-input NOR gate g303 which is controlled by a scan-enable signal line n301 and a signal line n302 with inverse polarity to the logic output is inserted. By forming in such a configuration, as compared with the first embodiment, the number of the gate stages present on the path from a system clock terminal to a logic output terminal can be reduced. In other words, the number of the gate stages on the path from the signal line to the logic output terminal is two stages in the first embodiment (the NOR gate g304 (in the conventional MUX-type scan FF, the scan-out terminal shown in Fig. 3 is the only output terminal) and the AND gate g104),

but there is only one stage (the NOR gate g303) in the present embodiment. Accordingly, by applying the present invention, the delay of the user logic circuit can be made smaller. Furthermore, since it is possible to reduce the size of the transistor forming the scan FF as compared with the first embodiment, the chip area reduction effect and the power consumption reduction effect can be expected.

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Fig. 7 is a timing chart showing the operation of the fifth embodiment. At the time of the transition from the scan-in operation to the logic test operation, it is possible to perform the release to fix the output signal to logic circuit, which is needed in the first embodiment, in parallel with the scan-in operation by setting the signal for fixing the output signal to logic circuit to "LOW" (s801) earlier than the scan-enable signal. For this reason, it becomes unnecessary to stop the clock signal transition (s802). Accordingly, there is an advantage that the test time can be reduced as compared with the first embodiment. Also, in the case of performing the burn-in test, the user logic circuit is operated with higher operating probability than that at normal operation. According to the present configuration, at burn-in, it becomes possible to operate the user logic circuit while inputting the signal to the scan FF.

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Fig. 17 is a diagram showing a flow for designing a semiconductor integrated circuit to which the present invention is applied. In this flow, an LSI design foundry implements the design in which the normal scan FF and the scan FF of the present invention are mixed (hereinafter, referred to as "mixed design by using this scan flipflop"). In the present embodiment, a client of LSI design provides the LSI design foundry with only the design specifications. In this diagram, the black thick line indicates a dependence relationship between the processing and the information, and the arrow of white blank indicates the flow of the information. Specifically, the LSI design foundry implements the mixed design by using this scan flipflop d2402 by using a design specifications d2401 provided by the client of LSI design, the cell library d1803 provided by a semiconductor foundry (performs the manufacture of the designed semiconductor integrated circuit), and the information of functional relationship between scan flipflop and normal flipflop d1804. Ultimately, the LSI design foundry prepares a gate-level netlist (hereinafter, referred to as "netlist using this scan flipflop") d2403. The

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prepared gate-level netlist d2403 is passed to the client of LSI design. In this respect, there will be a case where the cell library d1803 is also passed to the client of LSI design.

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Fig. 18 shows an example in which the LSI design foundry implements the mixed design by using this scan flipflop. In this embodiment, there is shown a handling in which the client of LSI design (also performs the manufacture of the designed semiconductor integrated circuit) provides the LSI design foundry with not only the design specifications but also the cell library, and the gate-level netlist. In this diagram, the black thick line indicates the dependence relationship between the processing and the information, and the arrow of white blank indicates the flow of the information. Specifically, the LSI design foundry implements the mixed design by using this scan flipflop d2402 by using the design specifications d2401, the cell library d1803, the information of functional relationship between scan flipflop and normal flipflop d1804 and the gate-level netlist not using the scan FF of the present invention (hereinafter, referred to as "netlist without this scan FF") d2501 all of which are provided by the client of